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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/736,720	12/16/2003	Keun Woo Lee	29936/39884	3564

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EXAMINER	
CHEN, ERIC BRICE	
ART UNIT	**PAPER NUMBER**
1765	

DATE MAILED: 08/08/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/736,720	LEE, KEUN WOO	
	Examiner	Art Unit	
	Eric B. Chen	1765	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 December 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9* is/are rejected.

7)☒ Claim(s) *1 and 6* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Priority

1. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Specification

2. The abstract is generally limited to a single paragraph on a separate sheet within the range of 50 to 150 words. It is important that the abstract not exceed 150 words in length since the space provided for the abstract on the computer tape used by the printer is limited.

Claim Objections

3. Claims 1 and 6 are objected to because of the following informalities: "pad oxide" apparently should be – pad nitride --. Otherwise, the claims 1 and 6 would be inconstant with the specification (Applicants' Specification, paragraph 0017) and the claim limitation of a "pad nitride" in claims 5 and 9 would lack the proper antecedent basis. Appropriate correction is required.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claims 1 and 6 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Specifically, use of the language "to the maximum extent" is vague because it is a subjective standard, which may have multiple interpretations.

6. Claims 2-5 are rejected under 35 U.S.C. 112, second paragraph, as being dependent on indefinite base claim 1.

7. Claims 7-9 are rejected under 35 U.S.C. 112, second paragraph, as being dependent on indefinite base claim 6.

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> **(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.**

9. Claims 1-4 and 6-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kunikiyo (U.S. Patent No. 6,495,424) in view of Wolf et al., *Silicon Processing for the VLSI Era*, Vol. 1, Lattice Press (1986), in further view of Rhodes et al. (U.S. Patent Appl. Pub. No. 2004/0178430).

10. As to claim 1, Kunikiyo discloses a method, comprising the steps of: forming a tunnel oxide film (2), a first polysilicon film (3) and a pad nitride film (4) on the semiconductor substrate (1), sequentially (column 14, lines 63-67; column 15, lines 1-3;

Figure 2); etching the pad nitride film (4), the first polysilicon film (3), the tunnel oxide film (2) and the semiconductor substrate (1) to form a trench (7) defining an active region and a device isolation region (column 15, lines 50-56; column 14, lines 6-11; Figure 1); forming a side wall oxide film on the side wall of the trench (8) (column 16, lines 16-23) while suppressing diffusion of ions for adjusting the threshold voltage into the device isolation region to the maximum extent (column 15, lines 30-36; column 21, lines 3-33; Figure 15); and forming a device isolation film by filling up inside the trench (7) (column 16, line 60; column 17, lines 37-42).

11. Kunikiyo does not expressly disclose performing an ion implantation process for adjusting a threshold voltage on a semiconductor substrate. Kunikiyo discloses doping of the region adjacent to the shallow trench isolation structure (column 14, lines 6-11). Wolf teaches that ion implantation is commonly used to introduce dopants into a semiconductor wafer in a precisely controlled manner. Moreover, the introduction of dopants into the semiconductor material inherently alters the threshold voltages (page 325). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to performing an ion implantation process for adjusting a threshold voltage on a semiconductor substrate. One who is skilled in the art would be motivated to dope the semiconductor by ion implantation, to introduce dopants in a highly controlled manner.

12. Kunikiyo does not expressly disclose performing an ion implantation process on the side wall of the trench and the active region adjacent to the device isolation region in order to compensate for ions for adjusting a threshold voltage which have diffused from

the active region into the side wall oxide film. Rhodes discloses a method (paragraphs 0015-0016), including performing an ion implantation process on the side wall of the trench and the active region adjacent to the device isolation region (paragraphs 0062-0063; Figure 14). Rhodes further teaches that implanting into the sidewalls and bottom of an isolation trench reduces surface leakage and reduces the dark current (paragraphs 0015-0016). Because Kunikiyo teaches that dopants may diffuse into the isolation structure (column 21, lines 14-33; Figure 15), one who is skilled in the art would expect that the ion implantation would compensate for ions for adjusting a threshold voltage which have diffused from the active region into the side wall oxide film. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to perform an ion implantation process on the side wall of the trench and the active region adjacent to the device isolation region in order to compensate for ions for adjusting a threshold voltage which have diffused from the active region into the side wall oxide film. One who is skilled in the art would be motivated to reduce the surface leakage and reduces the dark current of the isolation structure.

13. As to claim 2, Kunikiyo does not expressly disclose that the side wall oxide film is formed by a dry oxidation method at a temperature in the range of 800 °C to 950 °C. Wolf teaches that the conventional temperature range for the dry oxidation of silicon is a temperature in the range of 780 °C to 980 °C for the growth of thin oxides (pages 209-210). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the side wall oxide film by a dry oxidation method at a

temperature in the range of 800 °C to 950 °C. One who is skilled in the art would be motivated to select a conventional temperature, known to successfully produce an oxide film.

14. As to claim 3, Rhodes discloses that the ion implantation process is performed with a dose of 3×10^{11} ions/cm^2 to 1×10^{12} ions/cm^2 using an energy of 10Kev to 30Kev (paragraphs 0060-0061) at a tilt angle of 0° to 30° (paragraph 0046).

15. As to claim 4, Rhodes discloses that the implanted ion for adjusting the threshold voltage is boron (column 21, lines 3-10).

16. As to claim 6, Kunikiyo discloses a method comprising the steps of: forming a tunnel oxide film (2), a first polysilicon film (3) and a pad nitride film (4) on the semiconductor substrate (1), sequentially (column 14, lines 63-67; column 15, lines 1-3; Figure 2); etching the pad nitride film (4), the first polysilicon film (3), the tunnel oxide film (2) and the semiconductor substrate (1) to form a trench (7) defining an active region and a device isolation region (column 15, lines 50-56; column 14, lines 6-11; Figure 1); performing an annealing process for nitrifying a surface of the trench so as to form a nitride film (6) (column 15, lines 30-36) for preventing the ions for adjusting the threshold voltage from diffusing to the device isolation region (column 21, lines 3-33; Figure 15); forming a side wall oxide film on the side wall of the trench (8) (column 16, lines 16-23) while suppressing diffusion of the ions for adjusting the threshold voltage into the device isolation region to the maximum extent (column 15, lines 30-36; column 21, lines 3-33; Figure 15); and forming a device isolation film by filling up inside the trench (7) (column 16, line 60; column 17, lines 37-42).

17. Kunikiyo does not expressly disclose performing an ion implantation process for adjusting a threshold voltage on a semiconductor substrate. Kunikiyo discloses doping of the region adjacent to the shallow trench isolation structure (column 14, lines 6-11). Wolf teaches that ion implantation is commonly used to introduce dopants into a semiconductor wafer in a precisely controlled manner. Moreover, the introduction of dopants into the semiconductor material inherently alters the threshold voltages (page 325). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to performing an ion implantation process for adjusting a threshold voltage on a semiconductor substrate. One who is skilled in the art would be motivated to dope the semiconductor by ion implantation, to introduce dopants in a highly controlled manner.

18. Kunikiyo does not expressly disclose performing an ion implantation process on the side wall of the trench and the active region adjacent to the device isolation region in order to compensate for ions for adjusting a threshold voltage which have diffused from the active region into the side wall oxide film. Rhodes discloses a method (paragraphs 0015-0016), including performing an ion implantation process on the side wall of the trench and the active region adjacent to the device isolation region (paragraphs 0062-0063; Figure 14). Rhodes further teaches that implanting into the sidewalls and bottom of an isolation trench reduces surface leakage and reduces the dark current (paragraphs 0015-0016). Because Kunikiyo teaches that dopants may diffuse into the isolation structure (column 21, lines 14-33; Figure 15), one who is skilled in the art would expect that the ion implantation would compensate for ions for adjusting a

threshold voltage which have diffused from the active region into the side wall oxide film. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to perform an ion implantation process on the side wall of the trench and the active region adjacent to the device isolation region in order to compensate for ions for adjusting a threshold voltage which have diffused from the active region into the side wall oxide film. One who is skilled in the art would be motivated to reduce the surface leakage and reduces the dark current of the isolation structure.

19. As to claim 7, Kunikiyo does not expressly disclose that the side wall oxide film is formed by a dry oxidation method at a temperature in the range of 800 °C to 950 °C. Wolf teaches that the conventional temperature range for the dry oxidation of silicon is a temperature in the range of 780 °C to 980 °C for the growth of thin oxides (pages 209-210). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the side wall oxide film by a dry oxidation method at a temperature in the range of 800 °C to 950 °C. One who is skilled in the art would be motivated to select a conventional temperature, known to successfully produce an oxide film.

20. As to claim 8, Kunikiyo discloses that the annealing process is performed under N_2O atmosphere (column 15, lines 42-49). Kunikiyo does not expressly disclose that annealing process is performed at a temperature in the range of 800 °C to 900 °C. Wolf teaches that the conventional temperature range for the nitridation of silicon is a temperature in the range of 700 °C to 1200 °C for the growth of thin nitrides (page 210).

It should be noted that Applicants' claimed temperature range is within the conventional temperature ranges taught by Wolf. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to anneal at a temperature in the range of 800 °C to 900 °C. One who is skilled in the art would be motivated to select a conventional nitridation temperature, known to successfully produce a nitride film.

21. Claims 5 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kunikiyo, in view of Wolf, in further view of Rhodes, in further view of Song et al. (U.S. No. 6,635,532).

22. As to claims 5 and 9, Kunikiyo discloses eliminating the pad nitride film (4) (column 17, lines 55-56; Figure 10). Kunikiyo does not expressly disclose the remaining process steps. However, Song discloses a method of manufacturing a flash memory (column 3, lines 17-23), including forming a second polysilicon film (106) for a floating gate on the isolation structure (105) (column 4, lines 32-37; Figure 5A); forming a dielectric film (107) (column 4, lines 43-44) on the structure where the second polysilicon film (106) is formed (Figure 6A); and forming a third polysilicon film (108) for a control gate on the dielectric film (column 4, lines 49-53). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form a second polysilicon film for a floating gate on the structure where the pad nitride film is eliminated; form a dielectric film on the structure where the second polysilicon film is formed; and form a third polysilicon film for a control gate on the dielectric film. One

who is skilled in the art would be motivated to form a completed and functional flash memory device, using a previously successful method to form the device.

Conclusion

23. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Rhodes (U.S. Patent No. 6,177,333) discloses the ion implantation of an isolation trench in a semiconductor substrate. Shimizu (U.S. Patent No. 6,670,666) discloses the angled ion implantation of trenches.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eric B. Chen whose telephone number is (571) 272-2947. The examiner can normally be reached on Monday through Friday, 8AM to 4:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nadine G. Norton can be reached on (571) 272-1465. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

EBC

EBC
July 21, 2005

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SUPERVISORY PATENT EXAMINER